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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/904,622
Filing Date: July 13, 2001
Appellant(s): RENGAN ET AL.

Antony P. Ng
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 5/15/2006 appealing from the Office action mailed 3/29/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

Claims 1-7 and 24-37 are maintained and which were finally rejected by the Examiner as noted in the Final Office Action dated March 29, 2006 and in the advisory Action dated May 2, 2006, are being appealed.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5694141	CHEE	6-1995
5764201	RANGANATHAN	4-1996
5929871	KOMEICHI	4-1997

(9) **Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

3. Claims 1, 2, 4, 6, 7, 24-25, 27, 29-32, 34, 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chee (US 5,694,141) in view of Ranganathan (US 5,764,201).

Regarding claims 1, 24, 31, Chee discloses in figure 15, a method for providing displaying control on a computer system having a first display device (LCD 14) and a second display device (CRT 24), the method comprising allocating a first memory location (56) for storing contents to be displayed by said fist display device, wherein said first memory location is accessible by a video display controller (122), allocating a second memory location (56') for storing contents to be displayed by said second display device, wherein the second memory location is accessible by said video display controller; in response to a selection of a split display mode (see first and second display 14, 24; and first and second memory locations 56, 56'), retaining information in the first memory location and updating information in said second memory location (because the information is hold in the first memory location and after that will be changed information into second memory, therefore it means that the information in the first memory has updated in the second memory), such that contents displayed on said first display

device are different from contents displayed on the second display device (see col. 17, lines 45-54).

However, Chee does not disclose a concurrent display mode, providing identical information, such that contents displayed on the first display device are identical to contents displayed on the second display device.

Ranganathan discloses in fig. 10A, a concurrent display mode (see dual graphic controller in laptop PC 20 drives both display), providing identical information, such that contents displayed on the first display (CRT 24) device are identical to contents displayed on the second display device (LCD 22, see col. 10, lines 66-67, col. 11, lines 1-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the using of the identical information, such that contents displayed on the first display device are identical to contents displayed on the second display device as taught by Rangathan into the system of Chee having a first and second memories because this would provide to the user the identical images are displayed on the external CRT 24 and LCD panel 22 (see Rangathan, col. 11, lines 1-2).

Regarding claims 2, 25, 32, Chee providing information from a frame buffer (38, fig. 5) to the first and second memory locations (56, 56'). However, Chee does not disclose the identification information. Ranganathan discloses the identification in formation of fig. 10A, see col. 10, lines 66-67, and col. 11, lines 1-12 as discussed above.

Regarding claims 4, 27, 34, Chee discloses setting a pointer pointing from a frame buffer (66) to said first and second memory locations (56, 56'). However, Chee does not disclose the providing identical information. Ranganathan discloses the identification in formation of fig. 10A as discussed above.

Regarding claims 6, 29, 36, Chee discloses the first display device (CRT) is external from said computer system and the second display device (LCD) is internal to said commuter system (see fig. 5)

Regarding claims 7, 30, 37, Chee discloses the split display mode (two displays, two memories, discussed in claim 1) are made via a soft key function (see central processing unit CPU with input device and may run a program see col. 6, lines 26-33). However, Chee does not disclose a concurrent display mode. Rangathan discloses a concurrent mode in fig. 10A and discussed in claim 1.

4. Claims 3, 5, 26, 28, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chee (US 5,694,141) in view of Ranganathan (US 5,764,201) and in view of Komeichi (US 5,929,871).

Chee and Rangathan disclose every feature of the claimed invention, excluding the updating information further includes allocating a second frame buffer; and providing information from the second frame buffer to the second memory location while providing

information from the frame buffer to the first memory location; or the updating information further includes allocating second frame buffer and setting a second pointer pointing from said second frame buffer to the first memory location.

Komeichi discloses in figures 4-5 a second frame buffer (39); and providing information from the second frame buffer to the second memory (see second store region 39-2) location while providing information from the frame buffer (38) to said first memory location (see first store region 39-1); or the updating information further includes allocating second frame buffer (39) and setting a second pointer pointing from said second frame buffer (39-3) to said first memory location (see first store region 39-1) (see column 3, lines 35-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a second frame buffer; and providing information from said second frame buffer to said second memory location while providing information from said frame buffer to said first memory location as taught by Komeichi into the system having the first and second display of Chee and Ranganathan because this would improve the utilization efficiency of the memory capacity provided by memories forming the frame buffer part relatively simple circuit (see Komeichi, col. 4, lines 43-46).

(10) Response To Arguments

Appellant states that "the Examiner characterizes Chee's FIFOs 56 and 56'as a claimed first and second memory locations, respectively. According to Chee, "displays 14/24 and 14/24'

will each be supplied simultaneously with different display data. That is, the user of the computer system 10 will see a different image presented on the displays 14 and 24 simultaneously." However, the essence of simultaneously displaying different images on different displays does not necessarily mean "retaining information in said first memory location and updating information in said second memory location", as claimed.

Examiner respectively disagrees because the information is hold in the first memory location and after that the information will be transferred and changed into second memory, therefore it means that the information in the first memory has updated in the second memory, and after that, the contents displayed on said first display device are different from contents displayed on the second display device (see col. 17, lines 45-54).

Appellant also states that, 'the Examiner asserts that the teachings of the claimed allocation of two memory locations are also come from Chee. Chee depicts memory locations 100' and 120' along with FIFOs 56 and 56' to display different images on different displays. On the other hand, Ranganathan teaches one single memory 56 to provide to provide the same information to be displayed on two different displays. However, the Examiner has not indicated how Chee's teaching of two memory locations can be a applied to Ranganathan's teaching of a single memory. The Examiner has not provided any motivation or suggestions as to how Chee's method of displaying using two memory locations can be reconciled with Ranganathan's method of displaying using only one memory location to render the claimed invention obvious".

Examiner also respectively disagrees because Chee discloses a system comprising two memory locations 100' and 120' along with FIFOs 56 and 56' to display different images on different displays. However, Chee does not disclose a concurrent display mode, providing

identical information, such that contents displayed on the first display device are identical to contents displayed on the second display device. Ranganathan discloses a system having the concurrent display mode (see dual graphic controller in laptop PC 20 drives both display), providing identical information, such that contents displayed on the first display (CRT 24) device are identical to contents displayed on the second display device (LCD 22, see col. 10, lines 66-67, col. 11, lines 1-12). Thefore, the combination of Chee and Ranganathan are satisfied for its intended purpose.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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